Product Specification

Prouct:	**Bluetooth 4.0 BLE Module**
Module Number:	**CG-BT4GMD**
Doc Version:	**V1.3**
Data:	**September 3,2014**

Section 1:Overview

The CG-BT4GMD is a Bluetooth 4.0 module based on the Broadcom BCM20732 specification basic rate-compliant stand alone baseband processor with an integrated 2.4GHz transceiver.

The module includes EEPROM , crystal and PCB antenna.

1.1 Applications

The following profiles are supported in ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time

Additional profiles that can be supported from RAM include:

- Blood glucose monitor
- Temperature alarm
- Location

1.2 Features

- Bluetooth low energy (BLE)-compliant
- Supports Adaptive Frequency Hopping
- Excellent receiver sensitivity
- 10-bit auxiliary ADC with nine analog channels
- On-chip support for serial peripheral interface(SPI,UART) (master and slave modes)
- Programmable output power control
- Integrated ARM Cortex™-M3 based microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low-dropout regulator (LDO)
- On-chip software controlled power management unit
- Package type:20*13*2mm FR4 PCB with 25 pads located around the perimeter.
- RoHS compliant

1.3 Functional Description

The primary component on the module is the Broadcom BCM20732, which is a Bluetooth 4.0 compliant basic rate single-chip. The baseband and radio have been integrated into a single chip implemented in standard digital CMOS. The block diagram of the module is shown in Figure 1.

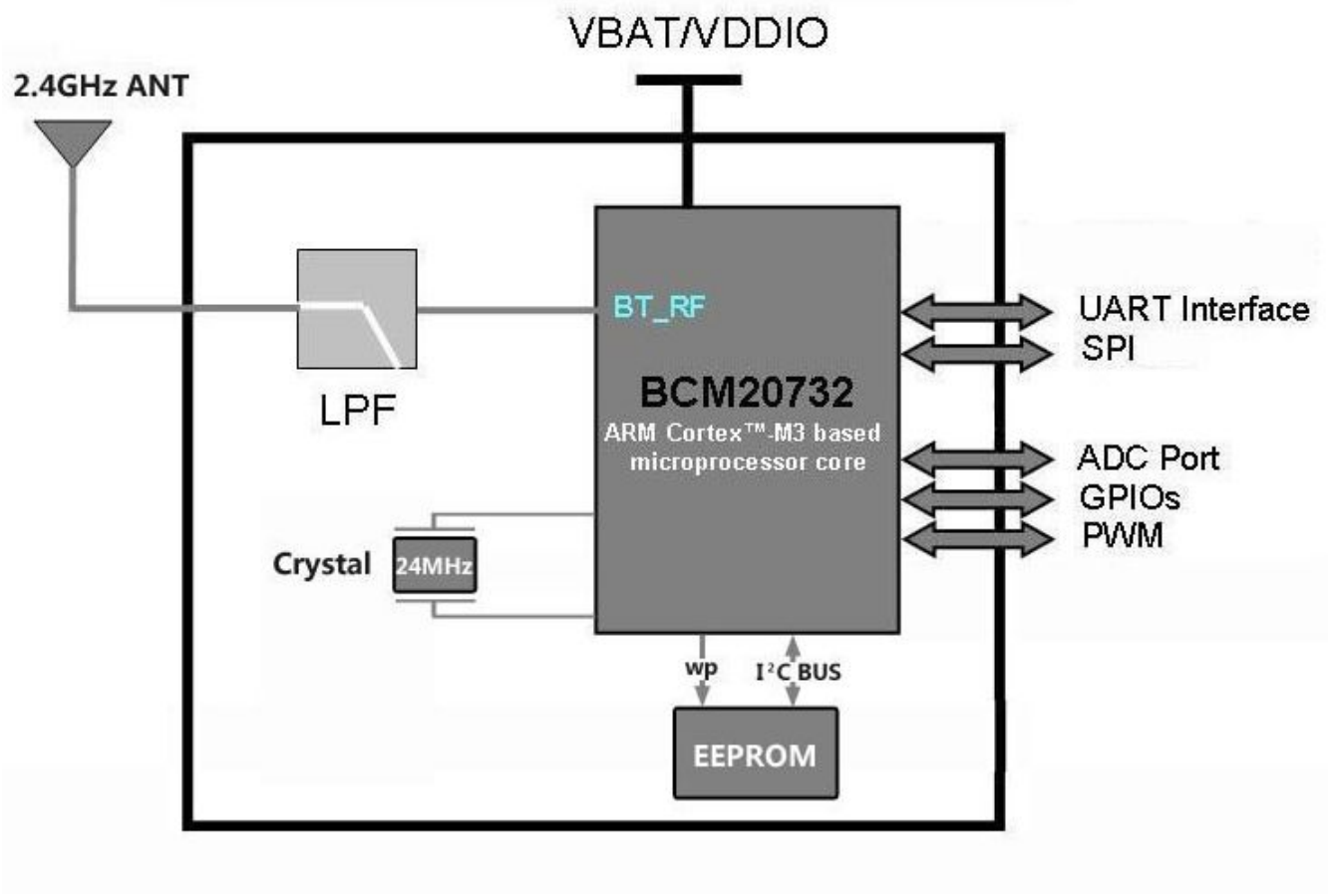


Figure 1: Block Diagram

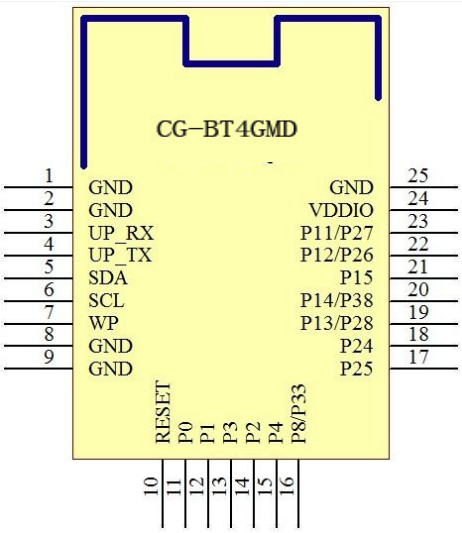
The CG-BT4GMD employs an integrated ARM Cortex™-M3 microprocessor core that runs software from the Link Control layer up to the Host Controller Interface (HCI).The baseband portion of the CG-BT4GMD performs all the time-critical functions required for high-performance Bluetooth operations.

The radio incorporates the complete receive and transmit paths, including PLL, VCO, LNA, PA, upconverter,downconverter, modulator, demodulator, and channel select filtering.

The module has a SPI interface. The interface has a 16-byte transmit buffer and a 16-byte receive buffer .To support more flexibility for user applications. The module acts as an SPI master device that supports 1.8V or 3.3V SPI slaves.

1.4 Physical Description

The CG-BT4GMD is a 20*13*2mm FR4 PCB with 25 pads located around the perimeter Fingle 2 shows the pinout diagram of the module.



Fingle 2 Pin Location

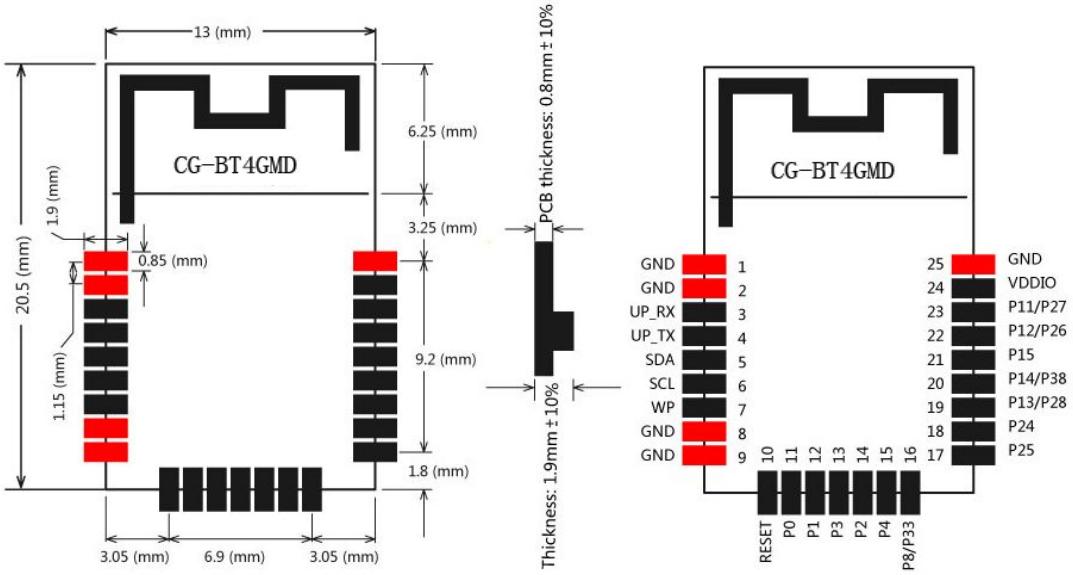


Figure 3 : Module PCB Layout Mechanical Specification

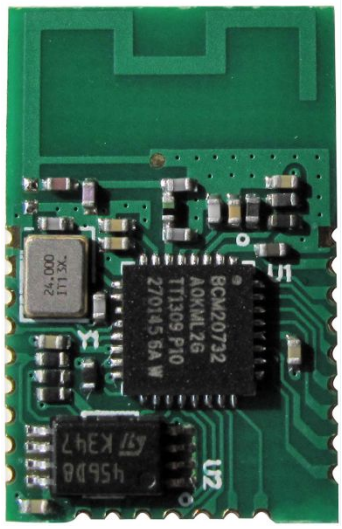


Figure 4 : Module PCB Top view

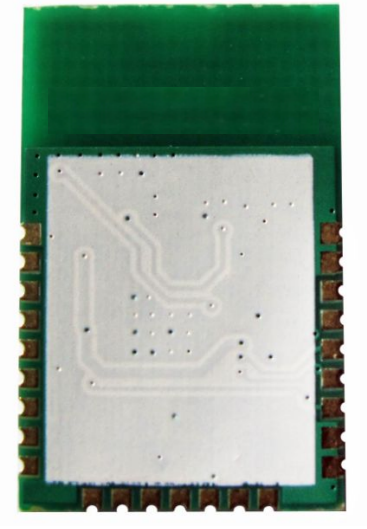


Figure 5 : Module PCB Bottom view

Table 1 shows the pin-out diagram of the module.

Table 1: Pin Description(Cont.)

Pin Number	Pin Name	Default State	Function Description
1,2,8,9,25	GND		Connect to ground
3	UP_RX	Input	UART input serial data for the HCI UART interface
4	UP_TX	output	UART output serial data for the HCI UART interface
5	SDA	I/ O	I2C Data
6	SCL	output	I2C Clock
7	WP	Input	Write protection
24	VDDIO		Power supply
10	RST		Active_low system reset
11	P0	Input floating	GPIO:P0 SPI_2:MOSI (master) A/D input
12	P1	Input floating	GPIO:P1 SPI_2:MISO (master) A/D input
13	P3	Input floating	GPIO:P3 SPI_2:CLK (master)
14	P2	Input floating	GPIO:P2 SPI_2:CS (master)
15	P4	Input floating	GPIO:P4
16	P8/P33	Input floating	GPIO:P8,P33 A/D input
17	P25	Input floating	GPIO:P25
18	P24	Input floating	GPIO:P24
19	P13/P28	Input floating	GPIO:P13,P28 A/D input PWM2
20	P14/P38	Input floating	GPIO:P14,P38 A/D input
21	P15	Input floating	GPIO:P15 A/D input(Battery moniter)
22	P11/P27	Input floating	GPIO:P11,P27
23	P12/P26	Input floating	GPIO:P12,P26

Section 2: Specifications

2.1 Electrical Characteristics

Table 2 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 2: Maximum Electrical Rating

Rating	Symbol	Value	Unit
DC supply voltage for RF domain	–		V
DC supply voltage for core domain	–	1.4	V
DC supply voltage for VDDM domain (UART/I2C)	–	3.8	V
DC supply voltage for VDDO domain	–	3.8	V
DC supply voltage for VR3V	–	3.8	V
DC supply voltage for VDDFE	–	1.4	V
Voltage on input or output pin	–	VSS – 0.3 to VDD + 0.3	V
Operating ambient temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–40 to +125	°C

Table 3 shows the power supply characteristics for the range T_J = 0 to 125°C.

Table 3: Power Supply

Parameter	*Minimum* [a]	*Typical*	*Maximum*[a]	*Unit*
DC supply voltage for RF	1.14	1.2	1.26	V
DC supply voltage for Core	1.14	1.2	1.26	V
DC supply voltage for VDDM (UART/I^2C)	1.62	–	3.63	V
DC supply voltage for VDDO	1.62	–	3.63	V
DC supply voltage for LDOIN	1.425	–	3.63	V
DC supply voltage for VDDFE	1.14	1.2[b]	1.26	V

a. Overall performance degrades beyond minimum and maximum supply voltages.
b. 1.2V for Class 2 output with internal VREG.

Table 4: Current Consumption [a]

Operational Mode	*Conditions*	*Typ*	*Max*	*Unit*
Receive	Receiver and baseband are both operating, 100% ON.	–	TBD	mA
Transmit	Transmitter and baseband are both operating, 100% ON.	–	TBD	mA
Sleep	Internal LPO is in use.	28.4	–	µA
HIDOFF	–	1.5	–	µA

a. Current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

2.2 RF Specifications

Table 5: Receiver RF Specifications

Parameter	*Mode and Conditions*	*Min*	*Typ*	*Max*	*Unit*
Receiver Section[a]					
Frequency range	–	2402	–	2480	MHz
RX sensitivity (standard)	0.1%BER, 1 Mbps	–	–85	–	dBm
RX sensitivity (low current)		–	TBD	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input	–	–10	–	–	dBm
Interference Performance[a,b]					
C/I cochannel	0.1%BER	–	–	21	dB
C/I 1 MHz adjacent channel	0.1%BER	–	–	15	dB
C/I 2 MHz adjacent channel	0.1%BER	–	–	–17	dB
C/I ≥ 3 MHz adjacent channel	0.1%BER	–	–	–27	dB
C/I image channel	0.1%BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	0.1%BER	–	–	–15	dB
Out-of-Band Blocking Performance (CW)[a,b]					
30 MHz to 2000 MHz	0.1%BER[c]	–	–30.0	–	dBm
2003 MHz to 2399 MHz	0.1%BER[d]	–	–35	–	dBm
2484 MHz to 2997 MHz	0.1%BER[d]	–	–35	–	dBm
3000 MHz to 12.75 GHz	0.1%BER[e]	–	–30.0	–	dBm
Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–55.0	dBm

a. 30.8% PER.
b. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
c. Measurement resolution is 10 MHz.
d. Measurement resolution is 3 MHz.
e. Measurement resolution is 25 MHz.

Table 6: Transmitter RF Specifications

Parameter	*Min*	*Typ*	*Max*	*Unit*
Transmitter Section				
Frequency range	2402	–	2480	MHz
Output power adjustment range	–	0	–	dBm
Default output power	–	4.0	–	dBm
Output power variation	–	2.0	–	dB
Adjacent Channel Power				
|M – N| = 2	–	–	–20	dBm
|M – N| ≥ 3	–	–	–30	dBm
Out-of-Band Spurious Emission				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	dBm
1.8 GHz to 1.9 GHz	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–47.0	dBm
LO Performance				
Initial carrier frequency tolerance	–	–	±150	kHz
Frequency Drift				
Frequency drift	–	–	±50	kHz
Drift rate	–	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence used is 00001111)	225	–	275	kHz
Maximum deviation in payload (sequence used is 10101010)	185	–	–	kHz
Channel spacing	–	2	–	MHz

2.3 Timing and AC Charactristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 7: UART Timing Specifications

Reference	*Characteristics*	*Min*	*Max*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

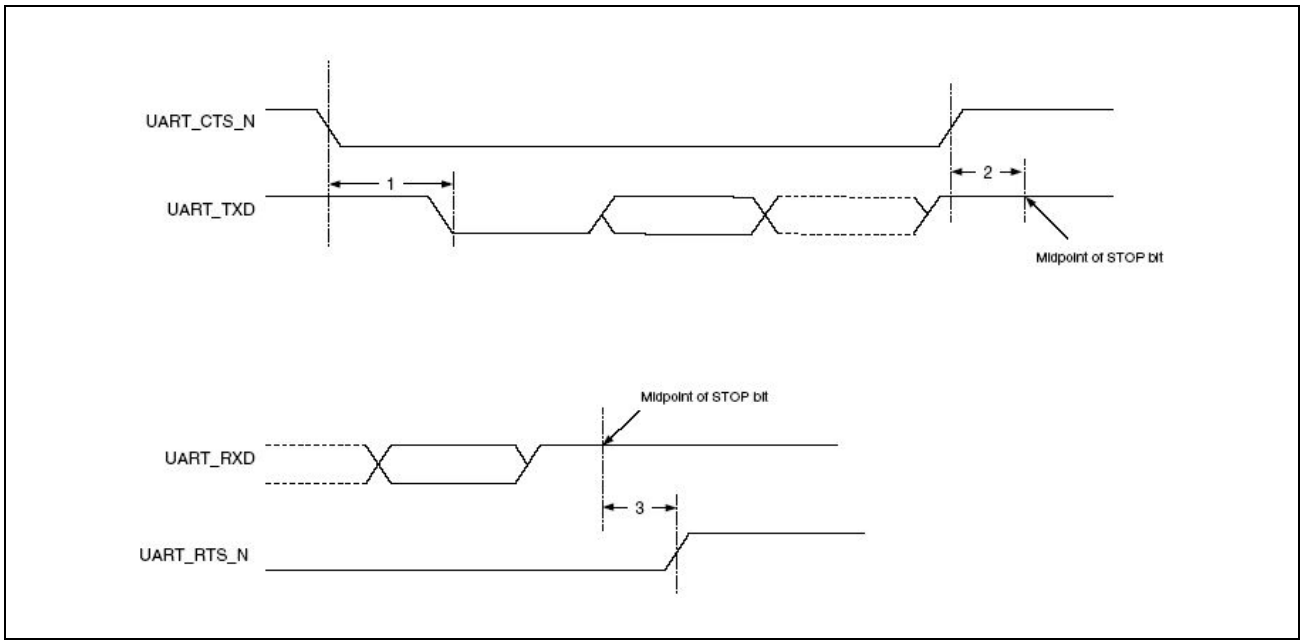


Figure 6: UART Timing

SPI Timing

The SPI interface supports clock speeds up to 12 MHz with VDDIO ≥ 2.2V. The supported clock speed is 6 MHz when 2.2V > VDDIO ≥ 1.62V.

Figure 7 and Figure 8 show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 8: SPI Interface Timing Specifications

Reference	*Characteristics*	*Min*	*Typ*	*Max*
1	Time from CSN asserted to first clock edge	1 SCK	100	∞
2	Master setup time	–	½ SCK	–
3	Master hold time	½ SCK	–	–
4	Slave setup time	–	½ SCK	–
5	Slave hold time	½ SCK	–	–
6	Time from last clock edge to CSN deasserted	1 SCK	10 SCK	100

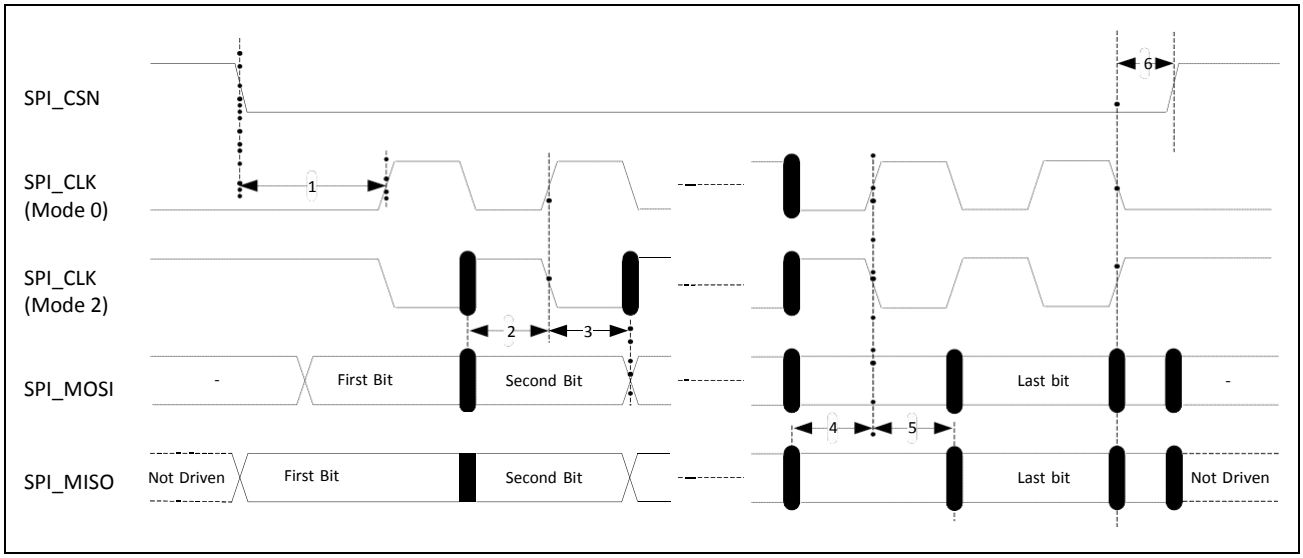


Figure 7: SPI Timing – Mode 0 and 2

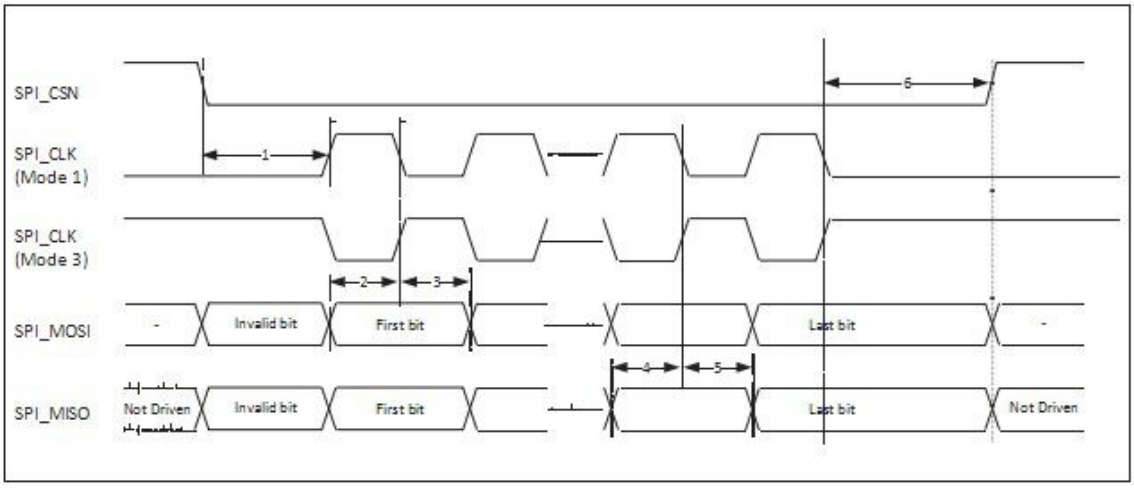


Figure 8: SPI Timing – Mode 1 and 3

Section3: Reference Design

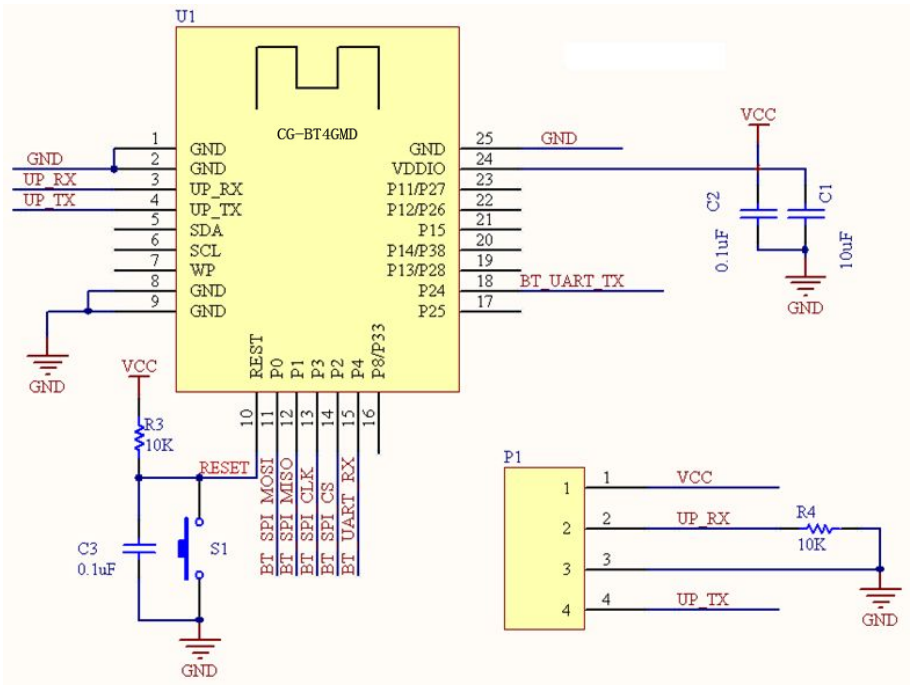


Figure 9: Module Reference Schematic

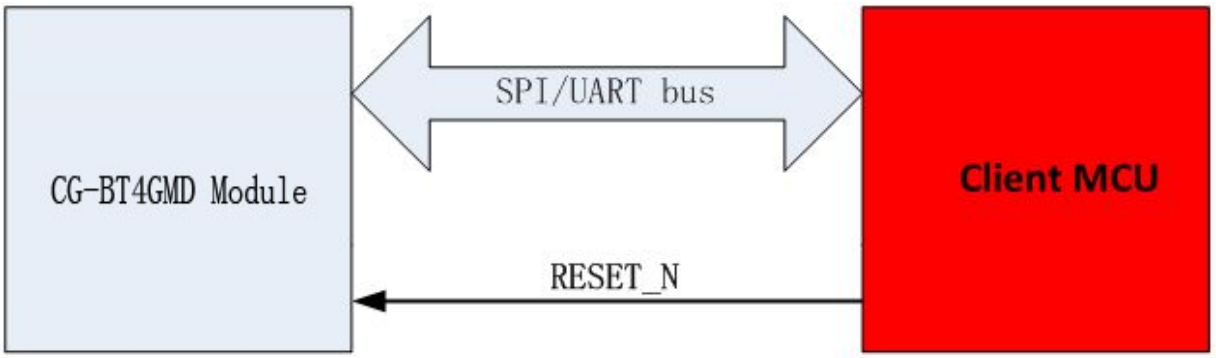


Figure 10: SPI/UART Reference Interface

REVISION HISTORY

Data	Revision	Changes
30-June-13	1.0	Initial Version
13-July-13	1.1	The position of Module pins is changed (1) Figure 2 is changed (2) Table 1 is changed (3) Figure 9 is changed
03-Sep-14	1.3	Figure 9 is changed Figure 10 is changed